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Fine Grain Dynamically Reconfigurable Architecture for CMOS Sram

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Abstract

Cell stability and area are among the major concerns in SRAM cell designs. This paper compares the performance of three SRAM cell topologies which include the conventional 6T-cell,8T-cell and 10T-cell. The cmos devices to achieve the better performance in terms of speed, power dissipation, size and reliability.SRAM(static random access memory)is memory used to store data. The comparison of different SRAM cell on the basis of different parameters is done.6T,8T and 10T SRAM cell are compared on basis of followings:1)Read delay, 2)Write delay, 3)power indulgence. The various SRAM solutions are analyzed in light of an impact on the required area overhead for each design solution given by Area(mm), Power(Mw) and delay(us). Different count of SRAM bitcells(6T, 8T, 10T) are analyzed. Among these 10T SRAM cell is better to immune SI (signal integrity), better STABILITY (Read + Write), Low Power consume bitcell. Inner architecture of FPGA OR CPLD comprised of No of CLB's interconnecting with inter-logics. (inter-logics like RAM contains SRAM bitcells are used connect the two CLB's inout)and One CLB contains no of slices . if one CLB comprised of 4 slice , it will communicate with one another using RAM like SRAM cells only

Keywords: Field programmable gate array(FPGA),logic folding, integrated circuits, Complementary (CPLD), complementary metal oxide semiconductor..

Introduction

As microprocessors and other electronics application get earlier and quicker, the need for large quantities of data at very high speed increases, while provided the data at such high speeds gets more difficult to accomplish. As microprocessor speed increases from 25MHz to 100MHz, to 250MHz and beyond, system designers have become more creative in their use of cache recollection, interleaving, burst mode and other prompt methods for accessing memory.

Static random access memory (SRAM) is a type of semiconductor memory that uses bi-stable latching circuitry to store each bit .The term static differentiates it from Dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits its data remanence,but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered.

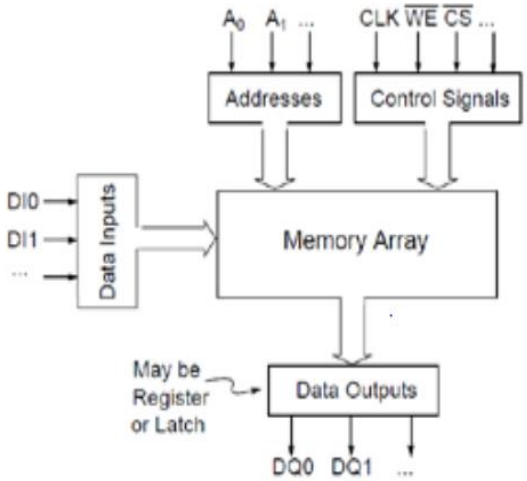

Fig.1.1 Block diagram of synchronous SRAM

Design of Sram Cells

Conventional 6t Sram

A different cell design that eliminates the above limitations is the use of a CMOS head over heels. In this case, the pack is replace by a PMOS transistor. This SRAM cell is composed of six

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transistors, one NMOS transistor and single PMOS transistor for each inverter, in addition two NMOS transistors connected to the row line. This cell offers better performance in speed and power than a 4T structure . Although this cell structure offers reduced area, its delay and power consumption are more compared to the 10T SRAM cell due to the absence of the readout inverter.

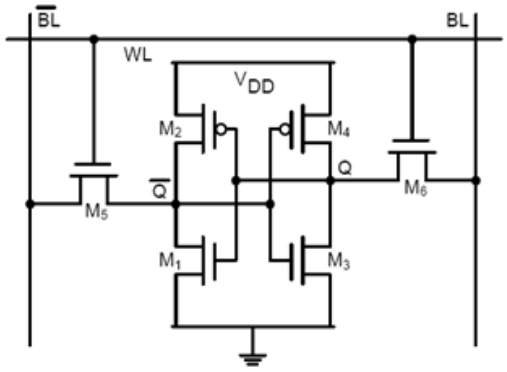

Fig 2.1 6T SRAM[7]

8T SRAM

An eight-transistor (8T) cell is proposed to improve variability tolerance and low-voltage operation in high-speed SRAM caches. While the cell itself can be designed for exceptional stability and write margins, array-level implications should also be considered to achieve a viable memory solution. These constraints can be addressed by modify traditional 6T-SRAM techniques and conceding some design complexity and area penalties. Altogether, 8T-SRAM can be considered without significant area penalty over 6T-SRAM while providing substantially improved variability tolerance and low-voltage operation with no need for secondary or dynamic power supplies.

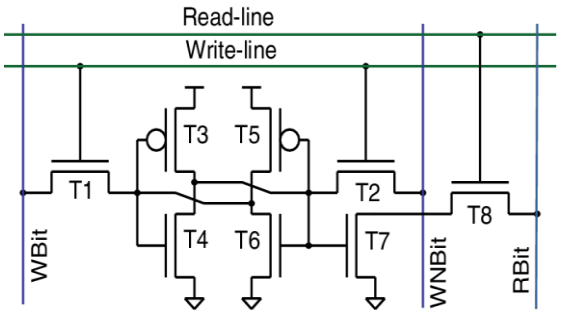

Fig.2.2 8T SRAM cell[7]

10T SRAM

A 10T SRAM cell includes a conventional 6T SRAM cell, a readout inverter and a transmission gate for the read port. These 10T SRAM cells enable both read and write operation. The write operation is same as achieved by a conventional 6T SRAM cell. For read operation, this 10T SRAM cell employs its non-pre charge scheme. Since the readout inverter is able to fully charge/ discharge the read bitline, the precharge scheme is not required. Therefore, the voltage on the bitline does not switch until the readout datum is changed and hence, the readout power is saved, also the delay is improved as well compared to conventional 4T and 6T SRAM cells, since the time for precharge is reduced. The area overhead of the cell relative to the conventional 6T SRAM cell and 4T SRAM cell is quite high. Since the 10T SRAM design avoids high switching activities on memory read bitlines and thus saves most of the charge/ precharge power, it is a promising candidate for low-power applications.

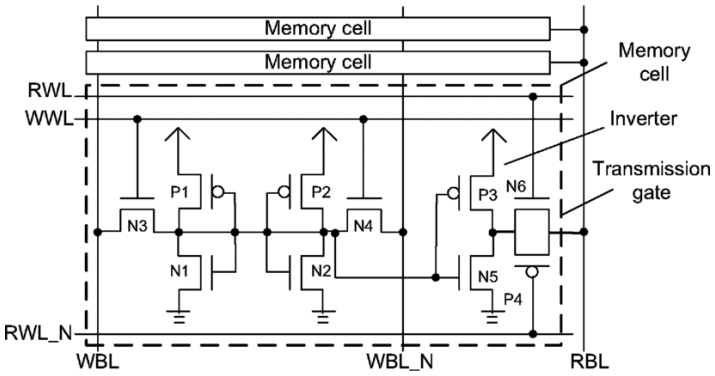

Fig.2.3 10T SRAM cell[1]

Virtual Hardware And Multicontext FPGAs

Recent dynamic reconfiguration FPGAs or CPLDs have made possible new varieties of reconfigurable systems or custom computing machines. In these system an algorithm is translated into FPGA configuration and executed directly. However a major obstacle has limited the use of these systems. The size of the variable FPGAs has restricted their application to small problems.

To address this problem, this paper proposed a data-driven virtual hardware system based on multicontext FPGA which provides multiple set of internal configuration SRAM .An algorithm to be executed described on a dataflow language and then translated into a dataflow graph. The graph is divided into a collection of FPGA contexts and executed into a data driven manner. Using a multiplexer, a particular context called the activated page is selected and corresponding configuration of logic is realized.

The capacity of multicontext FPGA can be extended by connecting the additional configuration of SRAM to offchip memory through a bus. while one

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configuration page is executing, we can load another one in parallel from the backup memory

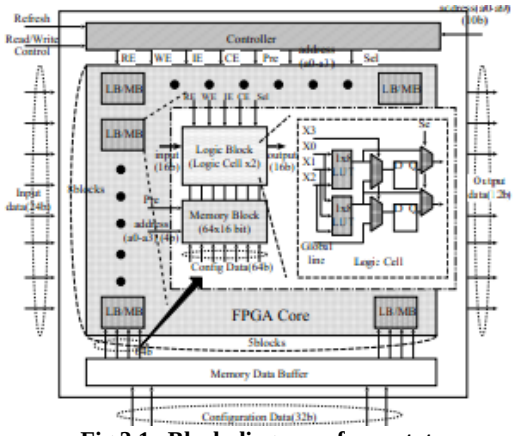

Fig.3.1 Block diagram of a prototype

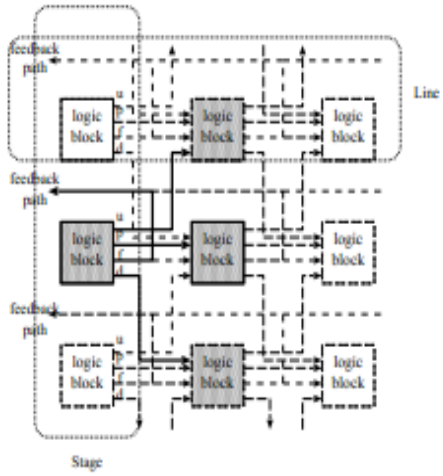

Fig 3.2 Connection between logic block

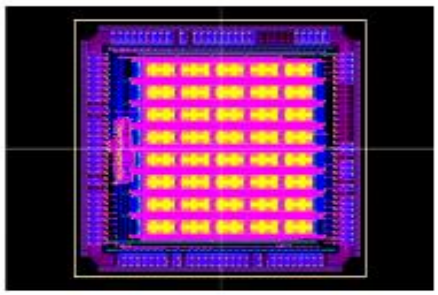

Fig 3.3 Layout of the Testchip

Chip Structure

The prototype chip consists of a logic block that contains logic cells,DRAM for configuration data and a controller. Each logic cell consists of two 1*8LUTs ,two DFFs and programmable multiplexers. A couple of LUTs corresponds to any 3-input/2-output logic is implemented, a 3 bit bus(X0,X1,X2) is used to address both the LUTs. On the other hand, when 4-input/1-output logic is required,X3 is used to select an output of the LUTs.This structure of a logic cell in which 3-input/2-logic output can be easily composed, makes it easy to build a data path component such as full adder. The chip structure is much flexible compared with FPGAs using coarse grain function logic cells (such as ALU).This logic block is designed to work with 100MHz clock.

Configuration memory is 64bit*16 line DRAM with MOS capacitance. The read operation of configuration data is done as follow. While a required memory line is selected by the address bus(A0-A3),CE(configuration enable) and RE(read enable) signals are asserted. The configuration data is loaded into the logic block and the logic realized in each logic cell is replaced at the same time. This context switch operation can be finished in one clock cycle. In each case, memory bit lines are needed to be precharged in advance.

Results and Conclusion

The final results for the area, delay and power dissipation as shown in fig 4.1

ANALYSIS

SI.NO	SRAM	NO.TR	DELAY(ns)	Power(watts)		
				average	max	min
1	6T	6	0.06	0.002618436	0.013652370	0.000000078
2	8T	8	0.25	3.460468e-004	1.541914e-002	7.187552e-006
3	10T	10	0.4	4.347430e-003	9.890540e-003	6.725722e-006

Fig.4.1 Analysis of delay and power

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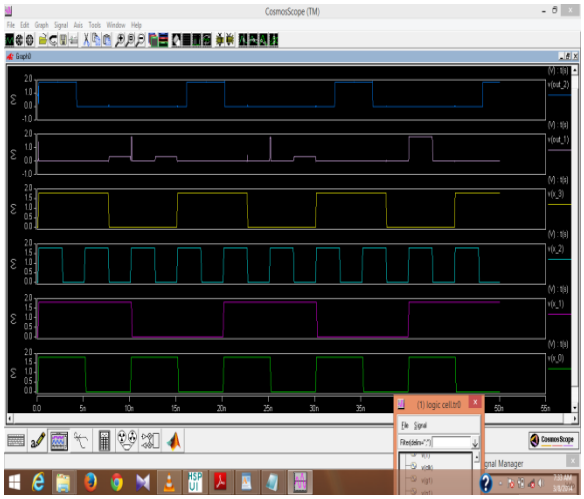

Fig 4.2 Simulated waveform of reconfiguration

Conclusion

The stability performances of the three SRAM cell topologies have been presented.fine-grain dynamically reconfigurable architectures for 6T, 8T, 10T be presented. All the beyond architecture uses low-power SRAM technology as storage for the configuration bits. Thus the simulation results of 6T, 8T and 10T have been exposed along with the associated phase diagram and compare by area, power and delay. The peripheral circuits of the SRAM architecture discussed were simplified to reduce power consumption.

In order to replace configuration contexts without stopping execution, level sensitive latches are required between the logic interface and SRAM sense amplifiers. The controller manages control signal such as RE,WE and CE and it is also used as an address decoder. The refresh operation of memory cells triggered by an external refresh signal. Once refreshing of cells is started, the execution is suspended until the refresh action is finished.

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